

Appl. No. 10/619,665  
Amndt. Dated: March 13, 2006  
Reply to Office Action of December 13, 2005

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### REMARKS

Claims 1-13 are pending in the Application, and claim 13 is withdrawn from consideration. Reconsideration and allowance of claims 1-12 are respectfully requested in view of the following remarks.

#### ***Claim Rejections Under 35 U.S.C. § 103***

Claims 1-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Choi, et al., U.S. Patent No. 5,608,558 (hereinafter "Choi") for the reasons stated on pages 2-4 of the Office Action. Applicants respectfully traverse the rejection.

For an obviousness rejection to be proper, the Examiner must meet the burden of establishing a prima facie case of obviousness. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). Establishing a prima facie case of obviousness requires that all elements of the invention be disclosed in the prior art. *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970).

Further, even assuming that all elements of an invention are disclosed in the prior art, an Examiner cannot establish obviousness by locating references that describe various aspects of a patent applicant's invention without also providing evidence of the motivating force which would have impelled one skilled in the art to do what the patent applicant has done. *Ex parte Levengood*, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. Int. 1993). The references, when viewed by themselves and not in retrospect, must suggest the invention. *In Re Skoll*, 187 U.S.P.Q. 481 (C.C.P.A. 1975). Here, all the elements are not disclosed in the prior art and even if combined, which there is no suggestion or motivation therefor, Applicant's invention does not result for the reasons set forth below.

The Examiner states that Katsumi teaches all of the elements of the above-mentioned claims, except that the test [pad] is formed on the TFT array panel, which the Examiner further states that it is well known to form test lines [on] the substrate at the same time of forming the TFTs in order to reduce the number of process/manufacturing steps required.

However, it is respectfully submitted that not only does Katsumi fail to disclose a test pad formed on the TFT array panel and connected to the inspection line, but Katsumi

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also fails to disclose an inspection line formed on the TFT array panel, contrary to the Examiner's position. More specifically, the Examiner states on page 2 of the Detailed Action that Kasumi teaches "an inspection line formed on the TFT array panel for receiving the test signals to the second display signal lines [see lines on TABs 9a and 9b] . . . ."

On the contrary, it is respectfully submitted that Katsumi teaches, with respect to FIG 7 relied upon by the Examiner, a defect detection apparatus including a flexible wiring substrate, namely a tape automated bondings (TABs") 8, 9a and 9b. TAB 8 connects odd-numbered gate lines (1) to terminal (A1) and even -numbered gate bus lines (1) to terminal (A2) on the TAB 8. The source bus lines (2) are connected through a common line to terminal (B) on TAB 9a. (Column 11, lines 1-8 of Katsumi).

Thus, Katsumi does not teach or suggest an inspection line formed on the TFT array panel for transmitting a test signal to the second display signal lines, and a test pad formed on the TFT array panel and connected to the inspection line, for receiving the test signal, as recited in claim 1. Therefore, claim 1, including claims depending therefrom, i.e., claims 2-11, define over Katsumi.

Further, it is respectfully submitted that the Examiner improperly equates the claimed limitation of "external devices" of claim 9 as being the external device on the flexible printed circuit films (9a), which the Examiner equates as the inspection lines for his claim analysis of claim 1. Thus, the Examiner inconsistently identifies the elements of Katsumi and improperly characterizes the same to read on Applicants' recited claim limitations.

To further support this assertion, the Examiner equates lines (13) as connecting lines for the rejections of claims 4 and 5, and then states for his rejection of claim 6 that Katsumi teaches the test pad is closer to an edge of the liquid crystal panel than to the connecting lines. It is further noted that the lines (13) of Fig. 7 of Katsumi are spare lines (13) connected to terminal D, and that Katsumi does not teach or suggest such lines (13) interconnecting the drivers, as recited in claim 4.

As stated above, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references

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themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP § 2143. As outlined above, the prior art does not teach all of the claim limitations, and thus, all three basic criteria have not been met. Therefore, the Examiner has not met the requirements for a *prima facie* case of obviousness.

Accordingly, it is respectfully requested that the rejection of claims 1-11 under § 103(a) be withdrawn and allow the same to issue.

#### **Conclusion**

In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance issued. If the Examiner believes that a telephone conference with Applicants' attorneys would be advantageous to the disposition of this case, the Examiner is cordially requested to telephone the undersigned.

In the event the Commissioner of Patents and Trademarks deems additional fees to be due in connection with this application, Applicants' attorney hereby authorizes that such fee be charged to Deposit Account No. 06-1130.

Respectfully submitted,

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